WHAT IS CLAIMED IS:

1. A liquid crystal display sequentially applying signal voltages based on display data to target pixels to display picture images at respective frames, comprising:

swing common electrodes for forming storage capacitors;

wherein voltages applied to said swing common electrodes are terminated with minus (-) during the period of gate on when the pixel voltages are inverted from minus (-) to plus (+), while being terminated with plus (+) when the pixel voltages are inverted from plus (+) to minus (-), and repeatedly swung from minus (-) to plus (+) after the gates turn off.

2. The liquid crystal display of claim 1, wherein an average pixel voltage V_p is given by following equation:

$$V_p = \pm V_s + (C_{st}/2(C_{st}+C_{gd}+C_{lc}))\cdot \Delta V_{com}$$

where V_s indicates voltage applied to a source terminal, C_{st} indicates capacitance of a storage capacitor, C_{gd} is parasitic capacitance between a gate terminal and a drain terminal, C_{lc} is capacitance of a liquid crystal capacitor, and ΔV_{com} is a difference between previous common voltage V_{com} and present common voltage V_{com}.

3. A liquid crystal display using swing common electrodes, comprising:

a timing signal control unit outputting a data driver driving signal and a gate driver driving signal, and also outputting first signals for defining cycle and amplitude of common voltages depending upon vertical synchronization signals, horizontal synchronization signals, and main clock signals applied from the outside;

a data driver outputting data driving voltages for driving polarities of a liquid

crystal capacitor based on the data driver driving signal;

a gate driver ouputting gate driving voltages based on the gate driver driving signal;

a driving voltage generation unit making the voltage level of the first signals to go up or down upon receipt of the first signals, and outputting swing common voltages synchronized with the gate driving voltages at a predetermined cycle; and

a liquid crystal display panel having one or more gate lines carrying scanning signals, one or more data lines crossing over the gate lines to carry picture signals, switching elements surrounded by the gate and data lines while being connected thereto, a liquid crystal capacitor transmitting light in proportion to the data driving voltages depending upon the turn on operations of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element, and applying the stored data driving voltage to the liquid crystal capacitor at the turn off of the switching element;

wherein the liquid crystal display panel is driven through a line inversion method such that the line at the present frame has a polarity inverted from the polarity of the line at the previous frame.

4. The liquid crystal display of claim 3, wherein the driving voltage generation unit outputs common voltages, the common voltage being terminated with minus (-) during the period of gate on in case the pixel voltage is inverted from minus (-) to plus (+) while being terminated with plus (+) when the pixel voltage is inverted from plus (+) to minus (-), and repeatedly swung from minus (-) to plus (+) after the gate turns off.

5. The liquid crystal display of claim 1, wherein an average pixel voltage V_p is given by following equation:

$$V_p = \pm V_s + (C_{st}/2(C_{st}+C_{gd}+C_{lc})) \cdot \Delta V_{com}$$

where V_s indicates voltage applied to a source terminal, C_{st} indicates capacitance of a storage capacitor, C_{gd} is parasitic capacitance between a gate terminal and a drain terminal, C_{lc} is capacitance of the liquid crystal capacitor, and ΔV_{com} is a difference between previous common voltage V_{com} and present common voltage V_{com}.

6. The liquid crystal display of claim 3, wherein the driving voltage generation unit outputs a first common voltage with the same width as a gate pulse when an odd numbered line is driven under the application of the gate pulse, and outputs a second common voltage with the same width as the gate pulse when an even-numbered line is driven under the application of the gate pulse.

7. The liquid crystal display of claim 3, wherein the driving voltage generation unit outputs a first common voltage with a pulse width k times longer than a gate pulse when the (n)th line is driven under the application of the gate pulse, outputs a second common voltage with a pulse width k times longer than the gate pulse when the (n+1)th line is driven under the application of the gate pulse, and outputs a third common voltage with a pulse width k times longer than the gate pulse when the (n+2)th line is driven under the application of the gate pulse.

8. A liquid crystal display using swing common electrodes, comprising:

a timing signal control unit outputting a data driver driving signal and a gate driver driving signal, and also outputting first signals for defining cycle and amplitude of

common voltages depending upon vertical synchronization signals, horizontal synchronization signals, and main clock signals applied from the outside;

a data driver outputting data driving voltages for driving polarities of a liquid crystal capacitor based on the data driver driving signals;

a gate driver ouputting gate driving voltages based on the gate driver driving signals;

a driving voltage generation unit making the voltage level of the first signals to go up or down upon receipt of the first signals, and outputting swing common voltages synchronized with the gate driving voltages at a predetermined cycle; and

a liquid crystal display panel comprising one or more gate lines carrying scanning signals, one or more data lines crossing over the gate lines to carry picture signals, switching elements surrounded by the gate and data lines while being connected thereto, a liquid crystal capacitor transmitting light in proportion to the data driving voltages depending upon the turn on operations of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element, and applying the stored data driving voltage to the liquid crystal capacitor at the turn off of the switching element;

wherein the liquid crystal display panel is driven through a dot inversion method such that the dot at the present frame has a polarity inverted from the polarity of the dot at the previous frame.

9. The liquid crystal display of claim 8, wherein the driving voltage generation unit outputs common voltages, the common voltage being terminated with minus (-) during the period of gate on when pixel voltage is inverted from minus (-) to

plus (+) while being terminated with plus (+) when pixel voltage is inverted from plus (+) to minus (-), and repeatedly swung from minus (-) to plus (+) after the gate turns off.

10. The liquid crystal display of claim 1, wherein an average pixel voltage V_p is given by following equation:

$$V_p = \pm V_s + (C_{st}/2(C_{st}+C_{gd}+C_{lc})) \cdot \Delta V_{com}$$

where V_s indicates voltage applied to a source terminal, C_{st} indicates capacitance of a storage capacitor, C_{gd} is parasitic capacitance between a gate terminal and a drain terminal, C_{lc} is capacitance of the liquid crystal capacitor, and ΔV_{com} is a difference between previous common voltage V_{com} and present common voltage V_{com}.

11. The liquid crystal display of claim 9, wherein the liquid crystal display panel further comprises a first common electrode line and a second common electrode line arranged between the neighboring gate lines in a horizontal direction, the first common electrode line connected to odd-numbered pixel electrodes, and the second common electrode line connected to even-numbered pixel electrodes.

12. The liquid crystal display of claim 11, wherein the driving voltage generation unit outputs a first common voltage with the same width as a gate pulse to the first common electrode line when the odd-numbered line is driven under the application of the gate pulse while outputting a second common voltage inverted in polarity against the first common voltage with the same width as the gate pulse to the first common electrode line when the even-numbered line is driven under the application of the gate pulse, and outputs the second common voltage inverted in polarity against the first common voltage to the second common electrode line with the

same width as the gate pulse when the odd-numbered line is driven under the application of the gate pulse while outputting the first common voltage with the same width as the gate pulse when the even-numbered line is driven under the application of the gate pulse.

13. The liquid crystal display of claim 11, wherein the driving voltage generation unit outputs a first common voltage with a pulse width k times longer than the gate pulse to the first common electrode line and the second common electrode line when the (n)th line is driven under the application of the gate pulse, outputs a second common voltage with a pulse width k times longer than the gate pulse to the first common electrode line and the second common electrode line when the (n+1)th line is driven under the application of the gate pulse, and outputs a third common voltage with a pulse width k times longr than the gate pulse to the first common electrode line and the second common electrode line when the (n+2)th line is driven under the application of the gate pulse.

14. The liquid crystal display of claim 11, wherein the liquid crystal display panel further comprises first and second common electrode lines provided between the data lines, the first common electrode lines being arranged at the odd-numbered vertical columns, the second common electrode lines being arranged at the even-numbered horizontal columns, the first and the second common electrode lines each having a storage capacitor formed at the crossed area of the gate and data lines with a predetermined volume so large as to co-act with the the liquid crystal capacitor.

15. The liquid crystal display of claim 11, wherein the first common

electrode line is odd-numbered and the second common electrode line is even-numbered, arranged in a horizontal direction.

odd-numbered gate lines arranged in the horizontal direction are positioned close to the odd-numbered common electrode lines,

even-numbered gate lines arranged in the horizontal direction are positioned close to the even-numbered common electrode lines;

odd-numbered data lines and even-numbered data lines are arranged in a vertical direction,

first storage capacitors are formed at the regions partitioned by the odd-numbered data lines and the even-numbered data lines while interconnecting the odd-numbered common electrode lines and the odd numbered gate lines close thereto. and

second storage capacitors are formed at the regions partitioned by the even-numbered data lines and the odd-numbered data lines while interconnecting the even-numbered common electrode lines and the odd numberedgate lines.

16. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with the same width as the width of a gate pulse to the odd-numbered common electrode lines under the application of the gate pulse, and outputs a common voltage of a second type with the same width as the width of a gate pulse to the even-numbered common electrode lines under the application of the gate pulse.

17. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width twice longer than the gate pulse to the (n)th common electrode lines under the application of the

gate pulse, outputs a common voltage of a second type with a pulse width twice longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, outputs a common voltage of a third type with a pulse width twice longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a fourth type with a pulse width twice longer than the width of a gate pulse to the (n+3)th common electrode lines under the application of the gate pulse.

18. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width three times longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second polarity with a pulse width three times longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a third polarity with a pulse width three times longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse.

19. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width five times longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second type with a pulse width five times longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, outputs a common voltage of a third type with a pulse width five times longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse, outputs a common voltage of a fourth type with a pulse width five

times longer than the gate pulse to the (n+3)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a fifth type with a pulse width five times longer than the gate pulse to the (n+4)th common electrode lines under the application of the gate pulse.

20. The liquid crystal display of claim 15, wherein the driving voltage generation unit outputs a common voltage of a first type with a pulse width three times longer than the gate pulse to the (n)th common electrode lines under the application of the gate pulse, outputs a common voltage of a second type with a pulse width three times longer than the gate pulse to the (n+1)th common electrode lines under the application of the gate pulse, outputs a common voltage of a third type with a pulse width three times longer than the gate pulse to the (n+2)th common electrode lines under the application of the gate pulse, outputs a common voltage of a fourth type with a pulse width three times longer than the gate pulse to the (n+3)th common electrode lines under the application of the gate pulse, outputs a common voltage of a fifth type with a pulse width three times longer than the gate pulse to the (n+4)th common electrode lines under the application of the gate pulse, and outputs a common voltage of a sixth type with a pulse width three times longer than the gate pulse to the (n+5)th common electrode lines under the application of the gate pulse.

21. The liquid crystal display of claim 11, further comprising:

a first pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as odd-numbered data lines and even-numbered data lines, said first pixel electrode having one end connected to the corresponding odd-numbered gate line and the other end connected to the

corresponding common electrode line;

a second pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the odd-numbered data lines and the even-numbered data lines, said second pixel electrode having one end connected to the corresponding even-numbered gate line and the other end connected to the corresponding common electrode line;

a third pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the even-numbered data lines and the odd-numbered data lines, said third pixel electrode having one end connected to the corresponding odd-numbered gate line and the other end connected to the corresponding common electrode line; and

a fourth pixel electrode formed at the regions surrounded by the odd-numbered gate lines and the even-numbered gate lines as well as the even-numbered data lines and the odd-numbered data lines, said fourth pixel electrode having one end connected to the corresponding common electrode line and the other end connected to the corresponding even-numbered gate line.

22. A method of driving a liquid crystal display, the liquid crystal display comprising a liquid crystal display panel having a gate line carrying scanning signals, a data line crossing over the gate lines to carry picture signals, a switching element surrounded by the gate line and the data line while being connected thereto, a liquid crystal capacitor transmitting light in proportion to data driving voltages depending upon states of the switching elements, and storage capacitors storing the data driving voltage at the turn on of the switching element and applying the stored data driving voltage to

the liquid crystal capacitor at the turn off of the switching element, the liquid crystal display being inversion-driven at each frame, the method comprising the steps of:

(a) checking variations in pixel voltages depending upon gate on and off operations of the switching circuits;

(b) outputting a common voltage terminated with minus (-) during a period of gate on while outputting a common voltage repeatedly swung from minus (-) to plus (+) during the period of gate off when the pixel voltage is inverted from minus (-) to plus (+); and

(c) outputting a common voltage terminated with plus (+) during a period of gate on while outputting a common voltage repeatedly swung from plus (+) to minus (-) during the period of gate off when the pixel voltage is inverted from plus (+) to minus (-).